

REMARKS

In the last Office Action, claims 8-17 were objected to because of informalities pointed out by the Examiner, and appropriate correction was required. Claims 8 and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by the newly cited reference to Sato. Claims 8 and 10-13 were rejected under 35 U.S.C. §102(b) as being anticipated by Ohshima. Claims 1, 6 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ohshima in view of Sudo. Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Sato in view of Sudo. Claims 2-5, 7 and 14-17 were objected to as being dependent upon a rejected base claim and were otherwise indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the informal objections.

Applicant and applicant's attorney acknowledge with appreciation the indication of allowability of claims 2-5, 7 and 14-17 and thank the Examiner for pointing out claim informalities which need correction.

In accordance with this amendment, claims 8 and 10 have been amended in the manner suggested by the Examiner to overcome the informal objections. In addition, independent claims 8 and 10 have been amended to further define the

interaction between the first and second output circuits. More specifically, claims 1 and 8 have been amended to recite that the first output circuit includes a MOS transistor and to recite, in the case of claim 1, that when the voltage across the battery is lower than a threshold voltage of the MOS transistor, the second output circuit outputs the second signal to maintain the first output signal of the output terminal and to recite, in the case of claim 8, that when the voltage across the input terminals is lower than a threshold voltage of the MOS transistor, the second output terminal has a low resistance value to maintain the first output signal of the output terminal. This is described in the specification, for example, on pages 7-8, 10 and 12-13.

The minor claim amendments made herein do not raise a new issue that would require further search or consideration. Instead, the claims have been amended to overcome the objections noted by the Examiner and to further define the interaction between the first and second output circuits, which were previously claimed. Applicant, therefore, respectfully requests entry of this amendment under the provisions of 37 C.F.R. §1.116.

The newly cited reference to Sato discloses a circuit for clearing a transistor when the power source exceeds the base-emitter saturation voltage of the transistor.

However, the Sato circuit does not have a second output circuit that assumes a low resistance value to maintain an output signal of the output terminal when the voltage across the input terminals is lower than a threshold voltage of a MOS transistor of a first output circuit, as specified in amended claim 8.

Likewise, Ohshima does not disclose the subject matter recited in amended claim 8. More specifically, in Ohshima, the second output circuit (R23, R22, Q11, Q12) does not assume a low resistance value to maintain a first output signal of the output terminal when the voltage across the input terminals is lower than a threshold voltage of a MOS transistor of the first output circuit 11c.

Therefore amended claim 8 and the claims dependent thereon are not anticipated by either Sato or Oshima, nor do the references render obvious these claims.

With respect to amended independent claim 1, the combined teachings of Oshima and Sudo do not teach a voltage detecting circuit wherein when the voltage across the battery is lower than a threshold voltage of a MOS transistor of the first output circuit, the second output circuit outputs the second signal to maintain the first output signal of the output terminal. While the Examiner has identified elements in the references that seemingly correspond to elements in the

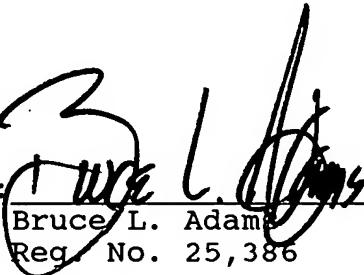
claim, the operation of the Oshima voltage detecting circuit, as modified by Sudo, does not function in the manner required by amended claim 1.

In view of the foregoing, the application is now believed to be in allowable form. Accordingly, favorable reconsideration and entry of this amendment together with passage of the application to issue are respectfully requested.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: MS AF, COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

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October 3, 2005

Date